REMARKS

Claims 1-2, 5-6, 9-10, 12-13, 15-16, and 19-20 are pending. Applicants have carefully considered the Office Action dated August 29, 2008 ("Office Action") in this Application. Applicants have amended Claim 1 in this Response. Applicants present the following remarks in a sincere attempt to place this Application in condition for allowance. Applicants respectfully request reconsideration and allowance in light of the above amendments and the following remarks.

Applicants thank the Examiner for the courtesy of an interview conducted November 13, 2008. During the interview the following remarks were discussed.

Applicants have amended Claim 1 in this Response to remove the words "the steps of." Applicants contend that the rationale underlying this amendment bears no more than a tangential relation to any rejection in question, nor do Applicants intend to surrender any equivalents encompassed by Claim 1 as a result of this amendment.

Claims 1-2, 5-6, 15-16, and 19-20 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 6,289,369 by Sundaresan et al. ("Sundaresan") in view of U.S. Patent No. 4,497,979 by Phelan ("Phelan"). Claims 9-10 and 12-13 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Sundaresan and Phelan in view of Willen and further in view of U.S. Patent No. 7,159,221 by Willen et al. ("Willen"). Applicants respectfully traverse these rejections. More particularly, Applicants respectfully submit that the Examiner's proposed combinations fail to teach each and every element as claimed, and in some cases directly contradict one or more elements as claimed.

First, in the present Office Action, the Examiner admits that "Sundaresan does not explicity teach each library processor comprise[s] exactly two task buffers." Office Action, Page 3. To supply this missing element, the Examiner offers Phelan as teaching "each library processor

comprise[s] exactly two task buffers", and asserting that "the first and second queue designated Q1 and Q2, respectively, have been defined in memory 300 associated with processor 301." Office Action, Pages 3-4 (*citing* Phelan, col. 5, lines 37-40). Applicants respectfully disagree with this assessment.

The Examiner's citation reads, in full: "In this illustrative embodiment of the invention a first and second queue designated Q1 and Q2, respectively, have been defined in memory 300 associated with processor 301." Phelan, col. 5, lines 37-40. But Phelan also states, exactly two lines down, "While only two queues are described in this embodiment it would be obvious to those skilled in the art that additional queues can be established for other classes of service depending on the needs of the system." Phelan, col. 5, lines 42-45. As such, Phelan clearly, and expressly, teaches away from "each library processor comprise[s] *exactly* two task buffers" (emphasis added).

The Examiner claims it would have been obvious to one of ordinary skill in the art "to incorporate the teaching of each library processor comprise exactly two task buffers as taught by Phelan because this allows to balance the system's overload conditions, service may be degraded to the point where delays in getting dial tone are experienced by the customers." Office Action, Page 4. Applicants respectfully note that nowhere is there any motivation to provide a telephone dial tone in the Sundaresan reference for "AFFINITY, LOCALITY, AND LOAD BALANCING IN SCHEDULING USER PROGRAM-LEVEL THREADS FOR EXECUTION BY A COMPUTER SYSTEM." Applicants respectfully object to the Examiner's stated motivation as insufficient and irrelevant.

Nevertheless, even if there were some motivation to add the ability to provide a dial tone to a customer to the Sundaresan system, which there is not, the Phelan system itself states that it would not be obvious to incorporate the teaching of exactly two task buffers, but rather "While only two

queues are described in this embodiment it would be obvious to those skilled in the art that additional queues can be established for other classes of service depending on the needs of the system." Phelan, col. 5, lines 42-45. Phelan itself disproves the Examiner's proposed combination—namely, that, according to Phelan, it is instead obvious to provide some number other than exactly two task buffers.

Additionally, as described in the Specification, there is a particular advantage to using exactly two task buffers:

> Since a library processor 108, 110, 112, 114, or 116 fetches tasks only when there is at most one task in the buffers, the load on a library processor is never more than two tasks, one of which is executing. As a result, the load is evenly balanced.

Original Application, Page 6, lines 9-14. In short, the Specification expressly teaches that there is an advantage to the invention as claimed, which advantage is expressly disavowed in Phelan. Applicants therefore respectfully submit that Phelan plainly teaches away from the Examiner's proposed combination. As such, for this reason alone, the Examiner's proposed combination fails to teach the very element the Examiner admits is missing from independent Claims 1, 9, and 15.

Moreover, Applicants respectfully submit that the Examiner's proposed combination also fails on at least two other elements. For example, in an earlier Action, the Examiner states: "Sundaresan does not explicitly teach at least one task from the plurality of tasks in the centralized task queue is distributed to at least one of the plurality of library processors when the library processor has at least one empty task buffer." Office Action dated Aug. 3, 2007, Page 3, Para 8. But in the current Office Action, the Examiner now asserts that Sundaresan teaches "wherein at least one task from the plurality of tasks in the centralized task queue is distributed tot [sic] at least

one of the plurality of library processors when the library processor has at least one empty task buffer." Office Action, Page 3 (citing Sundaresan, col. 8, lines 58-60).

The Examiner explains, "if there is no eligible thread in the per-processor local queue, then the thread from the central queue is dispatched for execution." Office Action, Page 3 (citing Sundaresan, col. 8, lines 58-60). But even if the Sundaresan per-processor local queue and central queue could be said to be adequate substitutes for the centralized task queue and the two task buffers per library processor as recited in the Claims, this does not prove that a task is distributed when the library processor has an empty buffer. At most, Sundaresan suggests that a task would be distributed when the two task buffers are full of ineligible threads, which is clearly distinct from "at least one *empty* task buffer" as recited in the claims. (emphasis added).

The Examiner also admitted in an earlier action that "Sundaresan does not explicitly teach . . . one of the plurality of library processors fetching the subtask from the centralized task queue," and offered Willen to show this element. Final Action dated Jan. 15, 2008, Page 3. The Examiner now asserts that Sundaresan does teach this missing element. *See* Office Action, Page 3. Specifically, the Examiner states, "the thread 22 remains in the schedule queue 26 until it is dispatched for execution by the scheduler." Office Action, Page 3 (citing Sundaresan, col. 7, lines 1-2; col. 8, lines 58-60). Applicants respectfully submit that this passage actually teaches away from the unique embodiments recited in the Claims.

Sundaresan states, "The thread 22 remains in the schedule queue 26 or 28 until it is *dispatched for execution by the scheduler 24*." Sundaresan, col. 7, lines 1-2 (emphasis added). Thus, the Examiner's citation expressly contradicts the plain language of the Claims, namely, "the library processors fetching the subtask from the centralized task queue." Instead of a library processor fetching tasks from a centralized queue, Sundaresan shows a central distributor scheduler

dispatching tasks to the processors, which is both contradictory to the claim language and precisely what the present invention seeks to avoid. *See, e.g.,* Original Application, Page 2 ("Therefore, there is a need for a method of load balancing in a multiprocessor system, that more evenly balances the load among the processors than traditional methods, *does not burden the central distributor*, and reduces the latency in task-loading." (emphasis added)). Here again, the Examiner's references expressly teach away from the proposed combination.

Accordingly, Applicants respectfully submit that independent Claims 1, 9, and 15 are therefore clearly and precisely patentable over Sundaresan, Phelan, Willen, and the remaining references of record, individually or in any combination. Therefore, Applicants respectfully request that the rejections of independent Claims 1, 9, and 15 be withdrawn and that independent Claims 1, 9, and 15 be allowed.

Claims 2 and 5-6 depend on and further limit Claim 1. Claims 10 and 12-13 depend on and further limit Claim 9. Claims 16 and 19-20 depend on and further limit Claim 15. As such, Applicants respectfully submit that these dependent Claims are also patentable over the cited references, individually or in any combination, for at least the reasons that their respective independent claims are patentable over the cited references, as described above. Accordingly, Applicants respectfully request that dependent Claims 2, 5-6, 10, 12-13, 16, and 19-20 also be allowed.

Applicants have now addressed all of the Claim objections and rejections cited in the Office Action. In view of the amendments to the Claims and Applicants' remarks, Applicants believe that pending Claims 1-2, 5-6, 9-10, 12-13, 15-16, and 19-20 are in condition for allowance, and respectfully request allowance of Claims 1-2, 5-6, 9-10, 12-13, 15-16, and 19-20.

Applicants believe no additional fees are due in this Response. In the event that any other fees are due, Applicants hereby authorize the Commissioner to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 09-0447 of IBM Corporation.

Applicants believe that the present Response contains a complete response to the issues raised in the Office Action. Applicants respectfully request full reconsideration. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, Applicants invite the Examiner to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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/Gregory W. Carr/
Gregory W. Carr
Reg. No. 31,093

CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003